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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,680	07/23/2003	Tetsuya Otsuki	116568	6686
25944	7590	08/04/2005	EXAMINER	
OLIFF & BERRIDGE, PLC P.O. BOX 19928 ALEXANDRIA, VA 22320			TRAN, LONG K	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Response to Amendment

1. This office action is in response to Amendment filed on July 05, 2005:
2. Claims **1 – 95, 98 – 104, 106 – 111** and **113** have been withdrawn from consideration.
3. Claim **96** has been amended.
4. Claims **96, 95, 105** and **112** are presented for examination.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims **96, 97** and **112** are rejected under 35 U.S.C. 102(b) as being anticipated by Wajnarowski et al. (US Patent No. 5,331,203).

7. Regarding claims **96** and **112**, Wajnarowski discloses semiconductor device 10 (fig. 1) comprising:

a substrate 12 (fig. 1(b)) including a depression (cavity) section 14 (fig. 1; column 9, lines 62 – 64), the depression 14 having an inner wall surface, the inner wall surface being curved or inclined respect to the substrate 12 (fig. 1);

a semiconductor chip 20 (fig. 1) mounted in the depression (cavity) section of the substrate with a surface of the semiconductor chip on which an electrode 24 (fig. 1) is formed facing upward (col. 10, lines 1 – 3);

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a first conductive layer 34 (fig. 1) formed over the substrate and the semiconductor chip so that the first conductive layer is electrically connected with the electrode 24 of the semiconductor chip (column 10, lines 8 – 12);

an insulating layer 36 (fig. 1; column 10, lines 61 and 62), at least a part of the insulating layer being disposed on the first conductive layer (figure 1);

and a second conductive layer 38, (fig. 1; column 11, lines 1 – 6) at least a part of the second conductive layer being disposed on the insulating layer over the first conductive layer 34.

Regarding claim 97, Wajnarowski discloses a polyetherimide resin layer formed in the depression section in which the semiconductor chip is mounted, wherein the first conductive layer is formed to pass over the resin layer (column 4, lines 25 – 60).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 105 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wajnarowski et al. (US Patent No. 5,331,203) in view of Gorowitz et al. (US Patent no. 5,524,339).

Regarding claim 105, Wajnarowski discloses the claimed invention of claim 96 but fails to teach a circuit board on which the semiconductor device is mounted.

However, Jeong discloses semiconductor device 30 (figs. 2 and 3) using metal patterns 32 of the circuit board 31 (figs. 2 and 3) as an external connection means (column 3, lines 48 – 57).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the device of Wajnarowski with the circuit board of Jeong, in order to increase the operational speed of the semiconductor chip using the circuit board as an external connection means (column 2, lines 1 – 5).

Response to Arguments

10. Applicant's arguments with respect to claims 96, 97, 105 and 112 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT



July 31, 2005



David Nelms
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